

## Contributing Authors

**Gunnar Braun** received his Diploma degree in Electrical Engineering from RWTH Aachen University in 2000. Since then, he published several technical papers and articles, and received the Best Paper Award at the Design Automation Conference in 2002. Mr Braun is one of the architects of the LISATek™ technology. Today, he is employed as a Principal Engineer at CoWare.

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**Matthias Gries** is a researcher at Infineon Technologies working on microarchitectures for network applications. He was a post-doctoral researcher with Prof. K. Keutzer at UC Berkeley from 2002 to 2004. He received his Ph.D. from ETH Zurich, Switzerland, in 2001 for his work on QoS network processors. His interests include methods for developing ASIPs, system-level design, and analysis of real-time embedded systems.

**Manuel Hohenauer** received the Diploma in Electrical Engineering from RWTH Aachen University in 2000 and is currently working towards the Ph.D. degree in Electrical Engineering at the same university. His research interests include retargetable code generation for embedded processors with main focus on machine description generation for retargetable compilers from architectural descriptions and retargetable code optimizations.

**Yujia Jin** received his B.S. degree in EECS at UC Berkeley in 1999. He is currently a Ph.D. student in the EE department at UC Berkeley. His research

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**David Kammler** received the Diploma degree in Electrical Engineering from the Institute for Integrated Signal Processing Systems, RWTH Aachen University, in 2003 where he is currently pursuing the Ph.D. degree. He is one of the architects of the RTL hardware generation from LISA focusing on integration of automatically generated processor features and the generation of memory and bus interfaces.

**Kurt Keutzer** received his B.S. degree in Mathematics from Maharishi International University in 1978 and his M.S. and Ph.D. degrees in Computer Science from Indiana University in 1981 and 1984 respectively. Kurt spent the first seven years of his career at AT&T Bell Laboratories and the next seven years at Synopsys, Inc. where he became Chief-Technical Officer and Senior Vice-President of Research. He then joined the Department of Electrical Engineering and Computer Science at University of California at Berkeley as a Professor. He has published five books, over one hundred refereed papers, and has been involved in the formation of several companies as both an investor and advisor.

**Chidamber Kulkarni** is a researcher in Xilinx Labs focusing on network processing. He was a post-doctoral fellow at UC Berkeley with Prof. Kurt Keutzer from 2001-2003 working on network processors. He was at the Belgium-based research center IMEC from 1997-2001, working on memory-centric design methodologies for embedded systems. Chidamber obtained a Ph.D. in electrical engineering from Katholieke Universiteit Leuven, Belgium in 2001.

**Steve Leibson** is the Technology Evangelist for Tensilica. He formerly served as Editor in Chief of the Microprocessor Report, EDN, and Embedded Developers Journal. He holds a B.S.E.E. from Case Western Reserve University and worked as a design engineer and engineering manager for leading-edge system-design companies including Hewlett-Packard and Cadnetix before becoming a journalist. Leibson is an IEEE Senior Member.

**Olaf Lüthje** received the Diploma degree in Electrical Engineering from RWTH Aachen University in 1997. In the following he worked there as a research assistant in the DSP tools group of the Institute for Integrated Signal Processing Systems (ISS). In 2003 he joined CoWare Inc. where he works in the devel-

opment team of the LISATek™ product family. In 2005 he received a Ph.D. degree.

**Grant Martin** is chief scientist at Tensilica, Inc., Santa Clara, California. He graduated with a Bachelor's and Master's of Mathematics from the University of Waterloo, Canada. He then worked at Burroughs in Scotland, BNR/Nortel in Canada, Cadence in San Jose, and has been with Tensilica for one year. His interests are in system-level design, SoC Design, and embedded systems.

**Heinrich Meyr** received his M.Sc. and Ph.D. from ETH Zurich, Switzerland. He spent over 12 years in various research and management positions in industry before accepting a professorship in Electrical Engineering at the RWTH Aachen University in 1977. He has worked extensively in the areas of communication theory, digital signal processing and CAD tools for system level design for the last thirty years. In 2001 he has co-founded LISATek Inc. In 2003 LISATek has been acquired by CoWare, an acknowledged leader in the area of system level design. At CoWare Dr. Meyr has accepted the position of Chief Scientist.

**Andrew Mihal** received his B.S.E.E. from Carnegie Mellon University in 1999. He is currently a Ph.D. candidate at UC Berkeley. His research interests include programming abstractions for embedded multiprocessors, and as a hobby, heuristic techniques for disguising seams in digital image mosaics.

**Matthew Moskewicz** is pursuing a Ph.D. in electrical engineering at the University of California, Berkeley. His research interests include satisfiability, formal modeling and languages for system design, and constraint based programming. Moskewicz has a BSE in electrical engineering from Princeton University. He recently joined CommandCAD, Inc.

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**Christian Sauer** heads the networked systems group at Infineon Technologies Corporate Research in Munich. After graduating from Dresden University of Technology in 1996 he joined Siemens CT labs working on processors for image processing, multimedia, and communications. From 2001-2004 he visited Prof. Keutzer's MESCAL group at UC Berkeley. His research interests are in ASIPs, SoC design, and embedded applications.

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**Niraj Shah** is a product marketing manager at Catalytic, Inc. in Palo Alto, Calif. He recently received a Ph.D. in electrical engineering and computer sciences from the University of California at Berkeley. His research focused on programming models for application-specific processors. Previously, Niraj was a venture partner at ITU Ventures, an early-stage venture capital firm investing in companies emerging from leading research institutions.

**Mel Tsai** received his M.S.E.E. in 2003 and is currently a 6th year Ph.D. candidate at UC Berkeley. Tsai has a B.S. in electrical engineering from Michigan State University. His dissertation work is called RouterVM, a novel configuration interface and architecture for next-generation network appliances.

**Scott Weber** is pursuing a Ph.D. in electrical engineering at the University of California, Berkeley. His research interests include tools and methods for the design and implementation of programmable platforms. Weber has a B.S. in electrical and computer engineering and a B.S. in computer science, both from Carnegie Mellon University.

**Andreas Wiefierink** received the Diploma degree in Electrical Engineering with honors from RWTH Aachen University in 2000. Since then, he is working toward the Ph.D. degree in Electrical Engineering at the same university. His current research interests include Multi-Processor System-on-Chips (MPSoC),

Retargetable Processor System Integration and Hardware/Software Cosimulation.

**Ernst Martin Witte** received the Diploma degree in Electrical Engineering in 2004 from the Institute for Integrated Signal Processing Systems, RWTH Aachen University, Germany, where he is currently pursuing the Ph.D. degree. Currently, his research focuses on architecture exploration and implementation of application specific processors based on LISA and an ADL based design flow aware of reconfigurable programmable architectures.